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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,234	03/16/2004	Fu-Hsin Chen	24061.79	2028

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EXAMINER

DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/801,234

Applicant(s)

CHEN ET AL.

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8-11 and 24-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 10, 11 and 26-29 is/are allowed.
- 6) ☒ Claim(s) 8 and 9 is/are rejected.
- 7) ☒ Claim(s) 24 and 25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/9/06 has been entered.

Claim Objections

2. Claim 24 is objected to because of the following informalities: In line 5 the wording "a substrate" appears to be a typo for "said substrate," as the wording "said substrate" would properly refer back to "a substrate" introduced in line 2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8 and 9 are rejected under 35 U.S.C. 92(b) as being anticipated by HOSHINO ET AL. (2001/0012671).

Hoshino et al. discloses a high-voltage MOS transistor comprising a substrate 1; a gate structure composed of a gate 7, a gate dielectric layer 6, and a gate spacer (the unnumbered cross-hatched region seen beside the unnumbered gate in figure 14a) overlying the substrate 1, the gate structure having a first side and a second side opposite to the first side; a first doping region 8 (Hoshino et al. call this the "offset region," as is common practice) with a first dosage formed in the substrate 1 on the first side of the gate structure and partially covered by the gate structure; a drain region (a second doping region 9 with a second dosage formed within the first doping region 8) adjacent to the edge on the first side of the gate structure; a source region (a third doping region 10 with the second dosage formed in the substrate 1) adjacent to the edge of the second side of the gate structure; and a channel region 5 formed in the substrate 1 between the first 8 and third 10 doping regions by turning on the high-voltage MOS transistor to pass current between the source 10 and drain 9 regions. Note figures 1, 14A and paragraphs 0135-0140 and 0211 of Hoshino et al.

Applicants are asked to next direct their attention to figures 32 and 36, and paragraphs 0256 and 0259 of Hoshino et al. In figure 32 Hoshino et al. show the on resistance increasing linearly with increasing gate (gate length being proportional to channel length) length. The slope of Hoshino et al.'s plot of on resistance versus gate

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length defines a resistance per unit length of Hoshino et al.'s channel region. In figure 36 Hoshino et al. show the on resistance increasing linearly with increasing offset region (Hoshino et al.'s "first doping region") length. The slope of Hoshino et al.'s plot of on resistance versus offset length defines a resistance per unit length of Hoshino et al.'s first doping region. Note that the two slopes are substantially equal. Hoshino et al. thus discloses that a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

Response to Arguments

4. Applicant's arguments filed 08/19/05 have been fully considered but they are not persuasive.

It is argued, at page 9 of the remarks, that "During a telephone interview, the examiner suggested that the photoresist pattern PR4 did the same 'function' as a gate spacer, as used in the patent. Applicants assert that we are talking about structure, not a method." The examiner either misspoke or his meaning was misunderstood. What the examiner intended to convey was that because, as seen in figure 14a, pattern PR4 prevents the arsenic implant (that creates second doping region 9) from reaching the substrate, the result is that second doping region 9 is offset from the gate structure by the exact width of pattern PR4, and the edge of second doping region 9 is exactly aligned with the edge of pattern PR4. Those having skill in the art would readily expect a "spacer" to be exactly aligned with the edge of a second doping region, and have a

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width identical to the distance by which the second doping region is offset from the gate. Further, those having skill in the art would expect a "spacer" to be capable of preventing an implant from reaching a substrate. See, e.g. figure 20 of Gasner 4599789, figure 6 of Pfister 4876213, figures 3 and 4 of Harrington 4906588, figures 9a-d (two pairs of spacers aligned with N+ as well as N++ source/drains) of Sanchez 5102815 (note that Sanchez also claims these unique spacers using "functional" language, figures 3e-3j of Ogoh 5254866, figures 4C-4G of Chau et al. 5783478, and figures 3A-3D of Akram et al. 5866460). The examiner did not mean to imply that Hoshino et al. disclosed any particular method. The examiner merely meant that Hoshino et al.'s patterns PR4 were capable of a particular functionality generally associated with spacers, and that when Hoshino et al. employed this functionality, a particular structure generally associated with spacers was created.

It is argued, at page 9 of the remarks, that "The photoresist pattern PR4 is not part of the gate structure to a person skilled in the art." However, patent claims construed during examination should be given their broadest reasonable interpretation consistent with Applicant's specification, and should be read in light of specification as it would be interpreted by person of skill in art, since this policy serves public interest by reducing possibility that claims, finally allowed, will be given broader scope than is justified (In re American Academy of Science Tech Center, 70 USPQ2d 1827, Decided May 13, 2004). The key words are "broadest reasonable interpretation," and "Applicant's specification." It does not matter what others might think the words "gate structure" mean. What

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matters is the meaning Applicant assigns to these words as conveyed by his claims and specification. See *Phillips v. AWH Corp.*, 75 USPQ2d 1321 (Fed. Cir. 2005) (*en banc*).

In the present case Applicant clearly states, in claim 9 (wherein the gate structure is composed of ... a gate spacer), that a proper part of a gate structure is a gate spacer. In applicants specification we are informed that a gate spacer (such as spacers 216 or 316) is formed on both sides of gates 214 or 314 (note paragraphs 13 and 27 and figures 2c and 3c) by etching a "conformable dielectric layer" (note paragraphs 15 and 29). This is all we are informed about Applicant's gate spacers. The broadest reasonable interpretation of "gate spacer," in light of this information, would include any spacer etched from a layer of conformable dielectric. Photoresist is inherently dielectric. See Lee et al. 5387495. Photoresist is inherently conformable and etchable. See Crivello 4537854. Within the broadest reasonable interpretation of a gate spacer formed by etching a conformable dielectric layer (which, applicant informs us, is part of a "gate structure") there is room for Hoshino et al.'s patterns PR4.

Allowable Subject Matter

5. Claims 10,11,26, and 27 are allowable over the prior art of record because they claim first and second doping (drain) regions having a range of implant dosages not disclosed or suggested by any prior art of record that also discloses or suggests a channel region with a resistance per unit length substantially equal to the resistance per

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unit length achieved by doping the first doping region with the first range of implant dosages.

6. Claim 24 is objected to for a minor informality (see section 2, above). Otherwise, claims 24,25,28, and 29 are allowable for the following reasons:

Each of these claims requires a channel region having approximately the same resistance per unit length as a first doping or “drain” region, said first doping or “first drain” region and a third doping or “source” region both being partially covered by a gate structure. As has been explained with respect to claims 8 and 9, Hoshino et al. 2001/0012671 discloses these elements. Hoshino et al. also discloses a first spacer in contact with the gate structure and covering a portion of the first doping or “first drain” region and offsetting it from a second doping region. However Hoshino et al. neither discloses nor suggests a second spacer in contact with the gate structure and covering a portion of the third doping or “source” region. Hoshino et al. discloses a second spacer, note figure 14a, but Hoshino et al.’s second spacer is not in contact (as required by claims 24,25,28, and 29) with the same gate structure as Hoshino et al.’s first spacer is in contact with.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Thomas L. Dickey', is positioned above the printed name and title.

Thomas L Dickey
Primary Examiner
AU2826
06/06